CPS-JK8

SHEET INDEX

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SYMBOL

BUS TERMINATOR A
ELEMENT IDENT
A

TERM. MOD	FUNCT	TERM.	LOC
ACKIO	I	115	2A4
BA16CRO	I	213	2A8
BACRO	I	300	2A7
BCLK	I	314	2A9
BBFLO	I	313	2A7
BSHPO	I	019	2A6
BSPARE	I	118	2A6
CLK	I	103	2A6
FILLO	I	316	2A9
GPO	I	202	2A5
IBO01	I	110	2A1
IBO11	I	109	2A1
IBO21	I	009	2A0
IBO31	I	010	2A0
IBO41	I	011	2A0
IBO51	I	111	2A0
INHBRO	I	201	2A8
INITO	I	114	2A4
RCO	I	216	2A2
ROO	I	007	2A2
SDINO	I	218	2A7
SDITO	I	018	2A7
SOO	I	016	2A3
SSTO	I	217	2A3
STUFFO	I	301	2A8
CLKRO	#	003	2M5
ERO	#	117	2M0
GBB1	#	004	2M8
GPRO	#	101	2M6
INTPO	#	302	2M1
ROYO	#	317	2M1
SYNCO	#	303	2M3
WAITO	#	104	2M7
+5	P	000,119	2M3
GRO	G	200,319	2M6

RECORD OF CHANGES

DWG ISS	PREV FURN	STO	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT ORAIN: 505mA

NOTES:

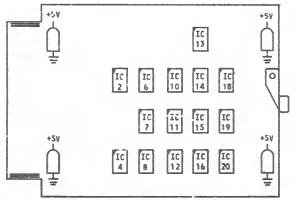
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRO TERM.
41AA	16	8
41AE	16	7,8
41BP	16	8
41BR	16	7,8
41CA	16	8
41U	16	8
41W	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS.

FUNCTION	TERMINAL
+5	000,119
GRO	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.
6. INTEGRATED CIRCUIT LOCATION GUIDE:
   (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK8
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE).	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

DWG ISSUE	ICE OR CO ISSUED	DATE ISSUE	Drawn	APPD
1	---	10-8-76	LRE	RWF MTS RFG
2D1	---	12-9-75	PSICE LRE	LEG RFG

ISSUE 2D1

IN98

JK8 CIRCUIT PACK

BUS TERMINATOR A CIRCUIT

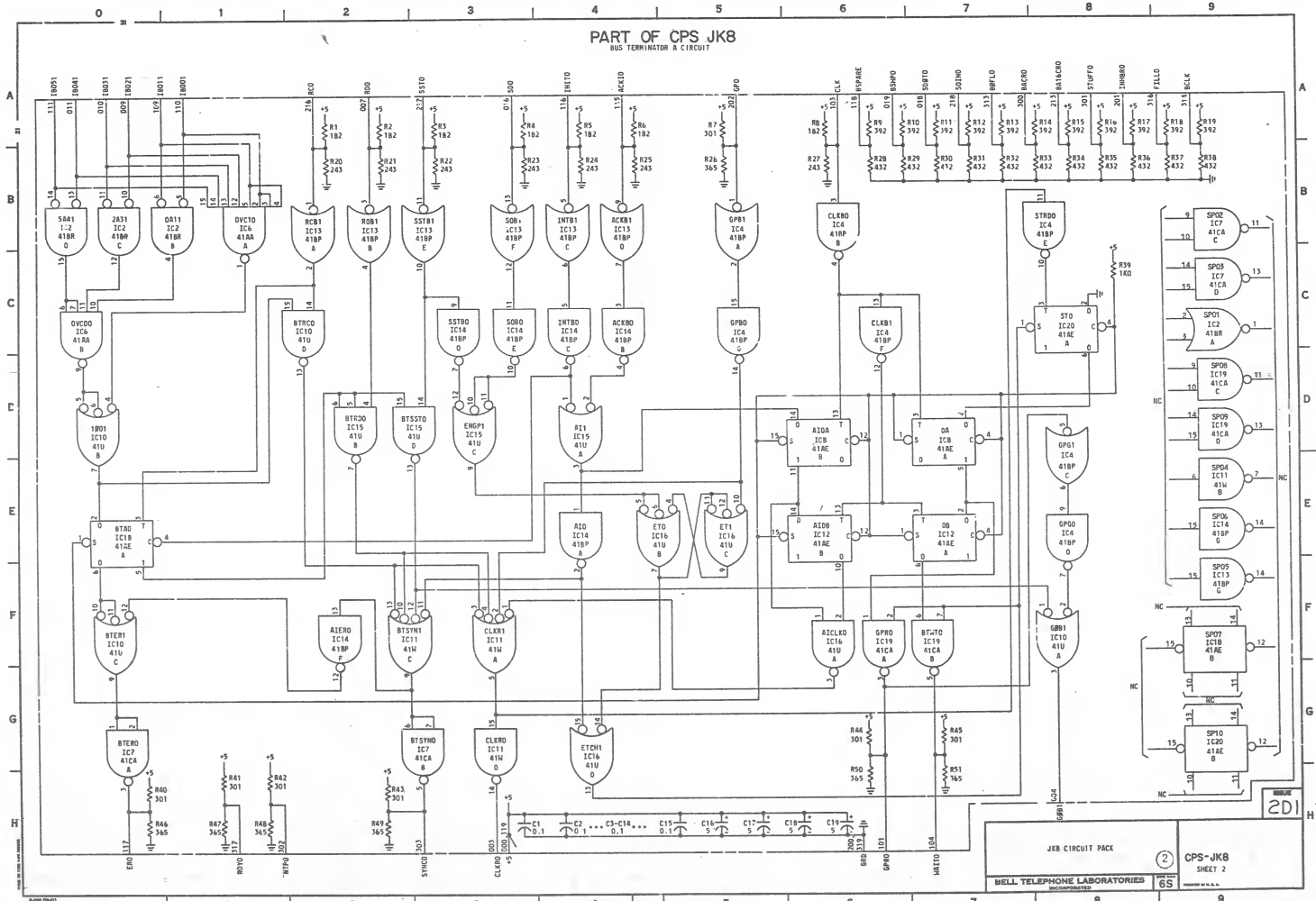
AT&TCO STANDARD

CPS-JK8
3 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

6S

CPS-JK8


PART OF CPS JK8
BUS TERMINATOR A CIRCUIT
JK8 CIRCUIT PACK
2
CPS-JK8
SHEET 2
BELL TELEPHONE LABORATORIES
INCORPORATED
6S
2D1
CPS-JK8

PART OF CPS JK8

BUS TERMINATOR A CIRCUIT

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC2 41BR DES1G	SH LOC	IC4 41BP DES1G	SH LOC	IC6 41AA DES1G	SH LOC	IC7 41CA DES1G	SH LOC	IC8 41AE DES1G	SH LOC	IC10 41U DES1G	SH LOC	IC11 41W DES1G	SH LOC	IC12 41AE DES1G	SH LOC	IC13 41BP DES1G	SH LOC	IC14 41BP DES1G	SH LOC	IC15 41U DES1G	SH LOC
A	SP01	2C9	GPB1	2B5	PVC10	2B1	BTER0	2G0	DA	2F7	GB01	2F9	CLKR1	2F3	DB	2E7	RCB1	2B2	AIO	2E4	AI1	2D4
B	OA11	2B1	CLKB0	2B6	DVC00	2C0	BTSYN0	2G3	AIDA	2D6	1B01	2D0	SP04	2E9	AIDB	2E6	RDB1	2B2	ACKB0	2C4	BTRD0	2D2
C	2A31	2B0	GPG1	2D9			SP02	2B9			BTER1	2F0	BTSYN1	2F2			INTB1	2B4	INTB0	2C4	ENGP1	2D3
D	SJ41	2B0	GPG0	2E9			SP03	2C9			BTRC0	2C2	CLKRD	2G3			ACKB1	2B4	SSTB0	2C3	BTSST0	2D3
E			STRD0	2B8													SSTB1	2B3	SDB0	2C3		
F			CLKB1	2C6													SDB1	2B3	AIER0	2F2		
G			GPB0	2C5													SP05	2F9	SP06	2E9		

LOC CODE ELEM ID	IC16 41U DES1G	SH LOC	IC18 41AE DES1G	SH LOC	IC19 41CA DES1G	SH LOC	IC20 41AE DES1G	SH LOC
A	AICLK0	2F6	BTAD	2E0	GPR0	2F6	STD	2C8
B	ET0	2E4	SP07	2F9	BTWT0	2F7	SP10	2D9
C	ET1	2E5			SP08	2D9		
D	ETCH1	2G4			SP09	2D9		
E								
F								
G								

CAPACITOR

DES1G	CODE
[15]C1-C15	KS-19774 L5,0.1
[4] C16-C19	601A,S

RESISTOR

DES1G	CODE
[6] R1-R6	KS-20616 L1A,182
R7	301
R8	182
[11]R9-R19	392
[6] R20-R25	243
R26	365
R27	243
[11]R28-R38	432
R39	1K0
[6] R40-R45	301
[6] R46-R51	365

CIRCUIT DESCRIPTION

THIS CIRCUIT PACK IS PART OF THE BUS TERMINATOR DEVICE. HANDSHAKING AND CONTROL LOGIC FOR THE PARALLEL HOLDING REGISTER ON JK9 IS PROVIDED. FAR-END TERMINATING RESISTORS FOR THE PARALLEL BUS COMMAND LEADS AND THE SERIAL BUS LEADS ARE ALSO PROVIDED.

THE BUS TERMINATOR ADDRESS FF (BTAD) BECOMES SET AT THE LEADING EDGE OF RCO AND IF 1B001 THROUGH 1B051 ARE ALL ONE'S OR ALL ZERO'S. RCB1 AND 1B01 ASSERT SYNCO AND CLKRO. SYNCO AND CLKRO REMAIN LOW UNTIL RCO RETURNS TO A HIGH LEVEL. AT THE TRAILING EDGE OF RCO, THE STATE OF THE INFORMATION LEADS IS CLOCKED INTO THE REGISTER ON JK9.

A LOW LEVEL ON RDO AND FF BTAD BEING SET ASSERTS SYNCO AND CLKRO. SYNCO REMAINS LOW UNTIL RDO RETURNS TO A HIGH LEVEL. AT THE TRAILING EDGE OF RDO, THE STATE OF THE INFORMATION LEADS IS CLOCKED INTO THE REGISTER ON JK9.

A LOW LEVEL ON SSTO AND FF BTAD BEING SET ASSERTS SYNCO AND GB01. GB01 GATES THE OUTPUTS OF THE REGISTER ON JK9 ONTO THE INFORMATION LEADS.

COMMAND INPUTS INITG OR ACKIO ASSERT SYNCO. WAITO IS ASSERTED BY ETCH1. FFS AIDA, AND GATE AICLK0 GENERATE A CLOCK PULSE ON CLKRO. THE TRAILING EDGE OF THIS PULSE CLOCKS THE STATE OF THE INFORMATION LEADS INTO THE REGISTER ON JK9. THE TRAILING EDGE OF CLKR1 TOGGLES FF STD ENABLING THE TIMING CHAIN. FFS DA AND DB TO ASSERT GPR0 AND GB01. WHEN FF DB BECOMES SET WAITO IS NEGATED. GPR0, GB01, AND SYNCO REMAIN TRUE UNTIL INITO OR ACKIO RETURN TO A HIGH LEVEL.

A PULSE ON THE GPO LEAD, WHILE SSTO OR SDO IS LOW, ENABLES THE TIMING CHAIN STD, DA, AND DB. THE LEADING EDGE OF GPO ASSERTS WAITO. AT THE TRAILING EDGE OF GPO, THE PARALLEL REGISTER ON JK9 IS CLOCKED VIA CLKR0 AND FF SID IS TOGGLED. THE NEXT TRANSITION OF THE CLOCK TOGGLES FF DA. THE ONE OUT-PUT OF FF DA ASSERTS GPR0 AND ENABLES THE OUTPUTS OF THE REGISTER ON JK9 VIA GOB1. THE NEXT TRANSITION OF THE INVERTED CLOCK (CLKB1) TOGGLES FF DB AND WAITO IS NEGATED. GB01 AND GPR0 REMAIN TRUE UNTIL SSTO OR SDO RETURN TO A HIGH LEVEL.

ISSUE 2D1

JK8 CIRCUIT PACK

BELL TELEPHONE LABORATORIES INCORPORATED

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